

# LabJack

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[Home](#) > [Support](#) > [Datasheets](#) > [U3 Datasheet](#) > [2 - Hardware Description](#) > [2.7 - DAC](#)

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## 2.7 - DAC [U3 Datasheet]

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### DAC Overview

The LabJack U3 has 2 analog outputs (DAC0 and DAC1) that are available on the screw terminals. Each analog output can be set to a voltage between about 0.04 and 4.95 volts with 10 bits of resolution (8 bits on older hardware revision 1.20/1.21). The maximum output voltage is limited by the supply voltage to the U3.

Starting with hardware revision 1.30 (2008), DAC1 is always enabled and does not affect the analog inputs, but with older hardware the second analog output is only available in certain configurations. With hardware revisions <1.30, if the analog inputs are using the internal 2.4 volt reference (the most accurate option), then DAC1 outputs a fixed voltage of  $1.5 \cdot V_{ref}$ . Also with hardware revisions <1.30, if DAC1 is enabled the analog inputs use  $V_{reg}$  (3.3 volts) as the ADC reference, which is not as stable as the internal 2.4 volt reference.

The DAC outputs are derived as a percentage of  $V_{reg}$ , and then amplified by 1.5, so any changes in  $V_{reg}$  will have a proportionate affect on the DAC outputs.  $V_{reg}$  is more stable than  $V_s$  (5 volt supply voltage), as it is the output from a 3.3 volt regulator.

The DACs are derived from PWM signals converted to DC with a 2nd order low pass filter. With the default timer clock of 48 MHz, the PWM frequency is 732 Hz and the output filter with a 16 Hz cutoff frequency works great. If the timer clock is lowered, which might be done for desired behavior on Timer0 & Timer1 ([Section 2.9](#)), the DACs will have more noise where the frequency of the noise is the timer clock frequency divided by 65536. This effect is more exaggerated with the 10-bit DACs on hardware revision 1.30+, compared to the 8-bit DACs on previous hardware revisions. The noise with a timer clock of 48/12/4/1 MHz is roughly 5/20/100/600 mV. If lower noise performance is needed at lower timer clock frequencies, use the power-up default setting in LJControlPanel to force the device to use 8-bit DAC mode (uses the low-level CompatibilityOptions byte documented in [Section 5.2.2](#)), since the PWM frequency is  $clock/256$  rather than  $clock/65536$ . A large capacitor (at least 220  $\mu F$ ) from DACn to GND can also be used to reduce noise.

Each channel of PWM hardware used to create the DACs has 2 bytes available to hold the duty cycle value. With 8-bit DACs the hardware will store the current value and new value, and switch over to the new value right at the start of a new cycle, thus assuring glitch-free operation. With

10-bit DACs this is not possible, and the new value is applied immediately. That means that on a DAC update to a new value a rising edge could be skipped, which would result in 1 cycle of all low, which after the filter would result in a glitch that looks like a negative going spike of perhaps 100-200 mV. If this is not acceptable use 8-bit DAC mode as mentioned in the previous paragraph.

The analog outputs have 2nd order low pass output filters with a 3 dB cutoff around 16 Hz, limiting the frequency of output waveforms to less than that, and corresponding to a step response time constant of about 10 ms. The reason for 16 Hz is that the cutoff frequency needs to be at least this low to filter the 732 Hz (default) PWM source to an acceptable DC output.

The analog output commands are sent as raw binary values (low level functions). For a desired output voltage, the binary value can be approximated as:

$$\text{Bits(uncalibrated)} = (\text{Volts}/4.95) * 256$$

For a proper calculation, though, use the calibration values (Slope and Offset) stored in the internal flash on the processor ([Section 5.4](#)):

$$\text{Bits} = (\text{Slope} * \text{Volts}) + \text{Offset}$$

The previous apply when using the original 8-bit DAC commands supported on all hardware versions. To take advantage of the 10-bit resolution on hardware revision 1.30, new commands have been added ([Section 5.2.5](#)) where the binary values are aligned to 16-bits. The calibration constants are still aligned to 8-bits, however, so the slope and offset should each be multiplied by 256 before using in the above formula.

The analog outputs can withstand a continuous short-circuit to ground, even when set at maximum output.

Voltage should never be applied to the analog outputs, as they are voltage sources themselves.

In the event that a voltage is accidentally applied to either analog output, they do have protection against transient events such as ESD (electrostatic discharge) and continuous overvoltage (or undervoltage) of a few volts.

There is an accessory available from LabJack called the [LJTick-DAC](#) that provides a pair of 14-bit analog outputs with a range of  $\pm 10$  volts. The LJTick-DAC plugs into any digital I/O block, and thus up to 10 of these can be used per U3 to add 20 analog outputs. The LJTick-DAC has various improvements compared to the built-in DACs on the U3:

- Range of +10.0 to -10.0 volts.
- Resolution of 14-bits.
- Slew rate of 0.1 V/ $\mu$ s.
- Based on a reference, rather than regulator, so more accurate and stable.
- Does not affect analog inputs in any configuration.

## 2.7.1 - Typical Analog Output Connections [U3 Datasheet]

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### 2.7.1.1 - High Current Output [U3 Datasheet]

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The DACs on the U3 can output quite a bit of current, but they have 50  $\Omega$  of source impedance that will cause voltage drop. To avoid this voltage drop, an op-amp can be used to buffer the output, such as the non-inverting configuration shown in [Figure 2-3](#). A simple RC filter can be added between the DAC output and the amp input for further noise reduction. Note that the ability of the amp to source/sink current near the power rails must still be considered. A possible op-amp choice would be the TLV246x family (ti.com).

### 2.7.1.2 - Different Output Ranges [U3 Datasheet]

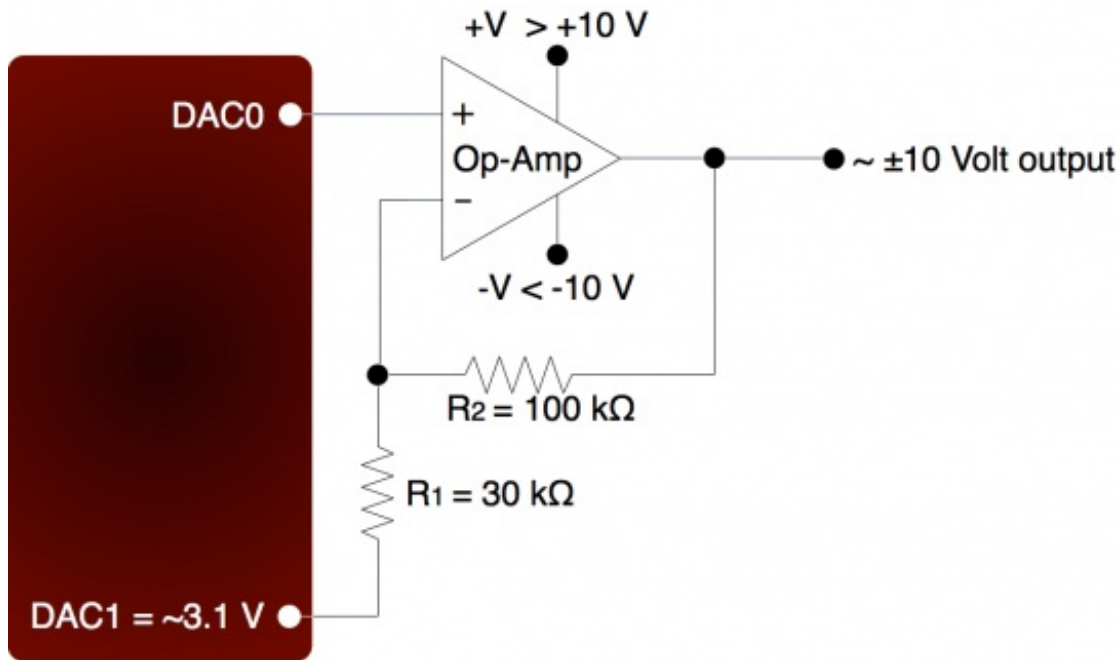
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See the end of this section for information about the [LJTick-DAC](#) which has a +/-10V range.

The typical output range of the DACs is about 0.04 to 4.95 volts. For other unipolar ranges, an op-amp in the non-inverting configuration ([Figure 2.6-1](#)) can be used to provide the desired gain. For example, to increase the maximum output from 4.95 volts to 10.0 volts, a gain of 2.02 is required. If R2 (in [Figure 2-3](#)) is chosen as 100 k $\Omega$ , then an R1 of 97.6 k $\Omega$  is the closest 1% resistor that provides a gain greater than 2.02. The +V supply for the op-amp would have to be greater than 10 volts.

For bipolar output ranges, such as  $\pm 10$  volts, a similar op-amp circuit can be used to provide gain and offset, but of course the op-amp must be powered with supplies greater than the desired output range (depending on the ability of the op-amp to drive its outputs close to the power rails). If  $\pm 10$ ,  $\pm 12$ , or  $\pm 15$  volt supplies are available, consider using the LT1490A op-amp (linear.com), which can handle a supply span up to 44 volts.

A reference voltage is also required to provide the offset. In the following circuit, DAC1 is used to provide a reference voltage. The actual value of DAC1 can be adjusted such that the circuit output is 0 volts at the DAC0 mid-scale voltage, and the value of R1 can be adjusted to get the desired gain. A fixed reference (such as 2.5 volts) could also be used instead of DAC1.



**Figure 2.7.1.2-1.**  $\pm 10$  Volt DAC Output Circuit

A two-point calibration should be done to determine the exact input/output relationship of this circuit. Refer to application note SLOA097 from ti.com for further information about gain and offset design with op-amps.

### **LJTick-DAC:**

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